WHAT IS CLAIMED IS:

Claim 1:

1. A circuit apparatus associated with a mid-level cache for handling side-door communal software lock (CSWL) inquiries in a multiple instruction-processor computer system comprising:

a. inquiry generator for generating signals containing either CSWL requests or status reports regarding locked status of a CSWL and for providing such inquiries and reports to another mid-level cache side door,

b. receiving circuit for receiving said CSWL inquiries and reports,

c. Interpreter for reading the signals in said CSWL inquiry to determine if it relates to a CSWL mapped to said associated mid-level cache and what each particular lock request function requires for any of said CSWL requests,

d. CSWL cache memory within said associated mid-level cache for storing CSWLs to which said associated mid-level cache is mapped, and means for determining if a CSWL which is subject to said CSWL inquiry is present within said CSWL cache memory,

e. comparator circuit for determining a current value of a requested CSWL within said mid-level cache's memory,

f. CSWL inquiry processor for processing said CSWL inquiry and for generating a response to said CSWL inquiry,

g. A circuit for responding to a requesting local processor with the status received from a status report.

Claim 2:

2. The circuit apparatus of claim 1 wherein said CSWL inquiry processor is said means for determining of part "d".

Claim 3:

3. The circuit apparatus of claim 1 wherein said CSWL inquiry processor includes said comparator circuit.

Claim 4:

4. The circuit apparatus of claim 1 further comprising a CSWL map directory for said associated mid-level cache containing addresses for each CSWL to which said associated mid-level cache is mapped and wherein said CSWL inquiry processor further comprises a circuit for determining whether a CSWL inquiry is mapped to said associated mid-level cache.

Claim 5:

5. The circuit apparatus of claim 4 further comprising a lock request generator for generating an inter-mid-level cache lock requests to send to other, non-associated mid-level caches if said CSWL inquiry processor determines a CSWL inquiry is not mapped to said associated mid-level cache.

Claim 6:

6. The circuit apparatus of claim 4 further comprising a lock request generator for generating an inter-mid-level cache lock requests to send a CSWL lock function to the CSWL data determined to be mapped to another, non-associated mid-level cache if said CSWL inquiry processor determines a CSWL inquiry is not mapped to said associated mid-level cache but is mapped to said non-associated mid-level cache.

Claim 7:

7. The circuit apparatus of claim 5 wherein said lock request generator for generating lock requests determines from information in said CSWL map directory which other, non-associated mid-level cache to which to direct said inter-mid-level cache lock request.

Claim 8:

8. The circuit apparatus of claim 1 further comprising a status stripper (?) circuit for fashioning a signal from a status field in a CSWL after processing by said CSWL inquiry processor to supply information needed to provide a reply to said CSWL inquiry.

Claim 9:

9. The circuit apparatus of claim 1 further comprising a side-door circuit for receiving said CSWL inquiries and status reports from other, non-associated mid-level caches having similar circuit apparatus to said claim 1 circuit apparatus through which to communicate with said other, non-associated mid-level caches said similar circuit apparatuses.

Claim 10:

10. The circuit apparatus of claim 8 wherein CSWL inquiries from processor units associated with said associated mid-level cache are received by said circuit apparatus through an internal data channel.

Claim 11:

11. The circuit apparatus of claim 1 wherein access to said lock cache is given a lower priority than access to a data cache in said associated mid-level cache.

Claim 12:

12. A computer system having a set of mid-level caches connected through said side door to side doors of said similar circuit apparatae in each of said non-associated mid-level caches, and wherein a radial communications pathway joins all such side doors.

Claim 13:

13. A computer system as set forth in claim 9 wherein the radial is a bus and the connection is a side door programmed to respond only to mapped CSWLs appearing on the bus.

Claim 14:

14. A computer system as set forth in claim 9 wherein the radial is a crossbar and the connections are configured by mapping of said CSWLs such that a given CSWL will map to a unique mid-level cache.

Claim 15:

15. A method for handling communal software locks (CSWLs) among a set of controller circuits situated in an associated set of mid-level caches in a multiprocessor computer system, comprising:

A) receiving a request for a software lock by a one of said set of controller circuits in a receiving one of said set of controller circuits (a receiving controller) from a requester,

B) interpreting said software lock request and if said interpreting yields a determination that said software lock request relates to a CSWL, then:

C) determining if said requested CSWL is mapped to said receiving controller and if mapped to said receiving controller:

1. searching said associated mid level cache for presence of said CSWL in said associated mid level cache,

2. if said requested CSWL is in a storage circuit in said associated mid level cache either:

a. setting said requested CSWL and returning an ownership indicia to said requester, or

b. if said requested CSWL is owned by another, returning a status to said requester,

3. if said requested CSWL is not in a storage circuit within said associated mid level cache:

a. forming a data request for the requested CSWL and sending said data request to said multiprocessor computer system to retrieve the requested CSWL from a current owner

b. receiving said requested CSWL from said multiprocessor computer system and processing said request in accord with sub-step 2, and

D) if said software lock request does not relate to a CSWL, passing said software lock request as ordinary data within said computer system.

Claim 16:

16. The method of claim 15 wherein step C 2) is performed by said receiving controller in said associated cache and wherein said requested CSWL is retained by said associated mid level cache.

Claim 17:

17. The method of claim 15 wherein said interpreting of step B comprises;

recognizing whether said request has been received into said associated mid level cache through a side door, and if received through said side door then determining that said request is a CSWL request.

Claim 18:

18. The method of claim 16 wherein said interpreting of step B comprises:

setting a flag indicator by a processor which uses said associated mid level cache to indicate that a software lock request is a CSWL request and recognizing said flag indicator by said receiving controller.

Claim 19:

19. The method of claim 15 further comprising prioritizing step C wherein step C will be performed by said set of mid level caches only after other mid level cache functions.

Claim 20:

20. The method of claim 15 further comprising prioritizing step C to be performed at a lower priority than other functions of said mid level cache, on an interleaved basis.